Enrollment No: _____ Exam Seat No:_____

C. U. SHAH UNIVERSITY

Winter Examination-2022

Subject Name: Analog and Digital Electronics

Subject Code: 4SC04ADE1 **Branch: B.Sc. (Chemistry, Mathematics)**

Semester: 4 **Date: 27/09/2022** **Time: 02:30 To 05:30** **Marks: 70**

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1		**Attempt the following questions:**	**(14)**
	a)	Draw circuit of AND gate using NAND Gates.	01
	b)	What is Amplifier?	01
	c)	What is CMRR in Op-AMP operation?	01
	d)	Define slew rate for OP-AMP.	01
	e)	Give full form of JFET.	01
	f)	Define pinch-off voltage.	01
	g)	Give the basic difference between analog and digital signal.	01
	h)	State applications of thermistor.	01
	i)	List the name of transistor biasing methods.	01
	j)	Write the truth table for NOR gate.	01
	k)	Give full form of UJT and draw its symbol.	01
	l)	Give Barkhahusen's criterion for self sustained oscillations	01
	m)	What is phase reversal?	01
	n)	Define voltage gain of amplifier.	01

Attempt any four questions from Q-2 to Q-8.

Q-2		**Attempt all questions**	**(14)**
	a)	Explain: Common Emitter Amplifier.	**07**
	b)	Explain any two applications of OP-Amp.	**07**
Q-3		**Attempt all questions**	**(14)**
	a)	Discuss in detail: Transistor as an amplifier in CB configuration.	**07**
	b)	Write a short note on OR Gate in details.	**07**
Q-4		**Attempt all questions**	**(14)**
	a)	Explain in details construction and working of MOSFET.	**07**
	b)	Explain in details construction and working of UJT.	**07**
Q-5		**Attempt all questions**	**(14)**
	a)	Give characteristics of ideal Op-Amp.	**08**

	b)	Explain in details NAND Gate as a universal gate.	**06**
Q-6		**Attempt all questions**	**(14)**
	a)	Explain in details NOT Gate with its logic circuit diagram.	**08**
	b)	Explain in details Half adder and Full adder circuits.	**06**
Q-7		**Attempt all questions**	**(14)**
	a)	Give truth table of XOR and XNOR Gates	**07**
	b)	Explain Integrator and Zero Crossing Detector using Op-Amps.	**07**
Q-8		**Attempt all questions**	**(14)**
	a)	Explain in details construction and working of JFET.	**08**
	b)	State and prove De Morgan's theorems.	**06**